ABSTRACT OF THE DISCLOSURE

A stagger type TFT substrate and a fabrication method therefor in which the number of exposure processes is reduced. A resist pattern is formed in an area on the TFT substrate where a drain bus-line (DB) is to be formed and an area on the TFT substrate where a TFT is to be formed by the use of a half tone mask. Etching is performed with this resist pattern as a mask to form the DB and a channel area for the TFT. In addition, a resist pattern is formed in an area where a gate bus-line (GB) is to be formed and an area where a pixel electrode is to be formed by the use of a half tone mask. Etching is performed with this resist pattern as a mask to form the GB and the pixel electrode. The DB and the channel are formed by one half tone mask and the GB and the pixel electrode are formed by another half tone mask. As a result, the number of exposure processes necessary for fabricating a stagger type TFT substrate can be reduced.